refreshing data based on a data charge retention time for the floating gate transistor that depends upon a barrier energy at an interface between the floating gate electrode and the gate insulator.

20. (Amended) The method of claim 19, wherein [storing data by changing the charge of the floating gate transconductively provides] reading data further comprises detecting an amplified current signal between the source and the drain.

21. (Amended) The method of claim 19, wherein the detected current is based on the charge of the floating gate electrode and a transconductance gain of the floating gate transistor.

28. (Amended) A method of using a floating gate transistor, comprising:

programming a floating gate electrode of the floating gate transistor by placing a charge on the floating gate electrode, wherein the floating gate transistor has a barrier energy[, defined as the difference between the electron affinity of the floating gate and the electron affinity of an] between the floating gate electrode and a silicon carbide (SiC) gate insulator separating the floating gate electrode from a substrate, [which is] the barrier energy being less than approximately 3.3 eV; and

reading the floating gate transistor by placing a read voltage on a control gate and detecting [the] current [conducted] in a channel between a source region and a drain region in the substrate.

29. (Amended) The method of claim 28[,] wherein programming the floating gate transistor further comprises causing hot electron injection from the channel through an amorphous silicon carbide (a-SiC) gate insulator to the floating gate electrode [the insulator includes amorphous silicon carbide (a-SiC)].

30. (Amended) The method of claim 28, [wherein the method further includes] further comprising erasing the floating gate transistor by applying an erase voltage to the floating gate transistor which is less than [12V] 12 Volts.

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31. (Amended) The method of claim 28, [wherein the method further includes] further comprising refreshing the charge placed on the floating gate electrode.

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32. (Amended) The method of claim 31, wherein refreshing the charge placed on the floating gate [includes] electrode further comprises refreshing the charge at regular time intervals of less than [40s] 40 seconds.

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33. (Amended) The method of claim 31, wherein refreshing the charge placed on the floating gate [includes] electrode further comprises refreshing the charge at regular time intervals [every few seconds].

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34. (Amended) A method for operating a floating gate transistor connected to a control line and a data line, the method comprising:

storing data on a floating gate electrode in the floating gate transistor by providing a control voltage on [a] the control line and a write voltage on [a] the data line such that charge is carried from a substrate to the floating gate electrode through [an] a silicon carbide (SiC) gate insulator, wherein a barrier energy between the silicon carbide (SiC) gate insulator and the floating gate electrode is less than 3.3 eV;

reading the data stored on the floating gate electrode by placing a read voltage on the control line and detecting the current [conducted through] in the floating gate transistor at the data line; and

erasing the floating gate transistor by applying an erase voltage to the floating gate transistor which is less than [12V] 12 Volts.

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35. (Amended) The method of claim 34[, wherein the insulator includes] wherein storing data further comprises causing the charge to be carried from the substrate to the floating gate electrode through an amorphous silicon carbide (a-SiC) gate insulator.

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36. (Amended) The method of claim 34, [wherein the method further includes] further comprising refreshing the charge placed on the floating gate electrode.

37. (Amended) The method of claim [32,] 36 wherein refreshing the charge placed on the floating gate [includes] electrode further comprises refreshing the charge at regular time intervals of less than [40s] 40 seconds.

38. (Amended) The method of claim [32,] 36 wherein refreshing the charge placed on the floating gate [includes] electrode further comprises refreshing the charge at regular time intervals [every few seconds].

Please add the following new claims 43-50:

43. (New) A method for operating a floating gate transistor comprising:

programming the floating gate transistor by inducing charge to migrate from a channel in a substrate through a silicon carbide (SiC) gate insulator to a floating gate electrode in the floating gate transistor; and

erasing the floating gate transistor by inducing charge to migrate from the floating gate electrode through the silicon carbide (SiC) gate insulator to the channel.

44. (New) The method of claim 43 wherein:

programming comprises programming the floating gate transistor by inducing hot electron injection from a channel in a substrate through an amorphous silicon carbide (a-SiC) gate insulator to a polysilicon floating gate electrode in the floating gate transistor; and

erasing comprises erasing the floating gate transistor by inducing charge to migrate from the polysilicon floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel through Fowler-Nordheim tunneling.

45. (New) The method of claim 43, further comprising reading the floating gate transistor by detecting current in the floating gate transistor.

46. (New) The method of claim 43, further comprising refreshing the floating gate transistor at regular time intervals.

47. (New) A method for operating a floating gate transistor connected to a control line and a data line, the method comprising:

programming the floating gate transistor by providing a control voltage on the control line and a write voltage on the data line to induce charge to migrate from a channel in a substrate through a silicon carbide (SiC) gate insulator to a floating gate electrode in the floating gate transistor; and

erasing the floating gate transistor by inducing charge to migrate from the floating gate electrode through the silicon carbide (SiC) gate insulator to the channel.

48. (New) The method of claim 47 wherein:

programming comprises programming the floating gate transistor by providing a control voltage on the control line and a write voltage on the data line to induce hot electron injection from a channel in a substrate through an amorphous silicon carbide (a-SiC) gate insulator to a polysilicon floating gate electrode in the floating gate transistor; and

erasing comprises applying an erase voltage of less than 12 Volts to the floating gate transistor to erase the floating gate transistor by inducing charge to migrate from the polysilicon floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel through Fowler-Nordheim tunneling.

49. (New) The method of claim 47, further comprising reading the floating gate transistor by placing a read voltage on the control line and detecting current in the floating gate transistor.

50. (New) The method of claim 47, further comprising refreshing the floating gate transistor at regular time intervals of less than 40 seconds.

REMARKS

In response to the Office Action mailed February 23, 1999, the applicant requests reconsideration of the above-identified application in view of the following remarks. Claims 19-21 and 25-42 are pending in the application, and claims 19-21 and 25-42 are rejected. Claims